UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,095	03/30/2001	Koichi Hashimoto	740250-837	2229

22204 7590 07/13/2005

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
DIVINE, LUCAS	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,095	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Lucas Divine	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1 – 5 are pending.

2. Specification and claim objections as well as 112 § first paragraph rejections have been withdrawn due to appropriate remarks and amendments.

Response to Arguments

3. Applicant's arguments filed 4/19/05 have been fully considered but they are not persuasive.

With respect to applicant's argument the decoder 136 outputs only one kind of data not both the unprocessed and processed input data.

In reply: Applicant admits (see bottom of page 6) and Examiner puts forth in Original Action (see item 5) that Lyons in col. 3 lines 40-42 teaches "the decode processor 136 receives and processes the delivered data stream S8 and passes the processed or unprocessed data stream S9 to the transmitter."

Applicant's limitation reads as: "at least one of the signal processor modules outputs both unprocessed input data and processed input data".

Lyon's decode processor can and does output both unprocessed and processed data as taught in the cited lines above.

To aid in understanding, as the claim currently stands, Examiner interprets broadly this limitation to read: "at least one of the signal processor modules outputs **(has the ability to output)** both unprocessed input data and processed input data".

Thus, the decode processor of Lyons clearly reads on the limitation and the rejection is maintained.

With respect to applicant's argument that Lyons teaches a STL (studio to transmitter link) and not an image processing apparatus.

In reply, the claim defines that an image processing apparatus comprises generally two processor modules where at least one module outputs both unprocessed and processed data. In this recitation of a image processing apparatus, the STL of Lyons can be considered an image processing apparatus. No limitation of the claim draws to any sort of image data or image processing – note what is claimed to be processed is 'data' and the modules are not claimed to do any sort of image processing steps specifically. Therefore the STL of Lyons reads on the prelude of claim 1 by teaching all claimed limitations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lyons (US 5903574).

Regarding claim 1, Lyons teaches **an image processing apparatus comprising at least two signal processor modules interconnected each other in series** (Fig. 2 modules 132 and 136 connected in series through a communication channel 134), **each of the signal processor modules having an input port through which data is input** (input ports by step S6 to module 132 and 136C for module 136), **a memory which stores data** (the operations involved in decoding and encoding inherently include some sort of memory to complete the operation on large portions of data over a period of time, e.g. registers, RAM), **a signal processor portion which carries out processing on input data according to program** (processing completed in 132B and 136B) **and an output port through which data is output** (output of module 132 by S7 and of module 136 by S9, both in Fig. 2), **wherein at least one of the signal processor modules outputs both unprocessed input data and processed data obtained by processing the input data** (col. 3 lines 40-42 discuss module 136 having the ability to output both unprocessed or processed data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyons in view of Ahamed et al. (US 5978831) hereafter referred to as Ahamed.

Regarding claim 2, which depends from claim 1, Lyons teaches all of the limitations of parent claim 1.

Lyons further teaches

said at least one of the signal processor modules 136:

stores unprocessed input data as input through the input port (decoder 136 implicitly stores the unprocessed data from the input 136C in order to perform the output of unprocessed data; col. 3 line 43) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (decoder 136 implicitly stores the processed data output by decoder 136B in order to perform the output of processed data; col. 3 line 42) **and**

outputs through the output port unprocessed data and processed data stored in the memory (col. 3 lines 40-43 teaches the outputting of unprocessed data and processed data stored in the decoder 136), **and**

the other signal processor module(s) 132:

stores in the memory unprocessed input data as input through the input port (encoder 132 implicitly stores unprocessed data in order to perform processing on it as discussed in the rejection of claim 1) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (encoder 132 implicitly stores processed data and processes the data by reading from the implicit memory, processing, and writing back to memory as standard processing technique known to those of ordinary skill in the art; processing discussed in col. 3 lines 31-36) **and**

outputs through the output port processed data stored in the memory (Fig. 2 by S7, encoder module 132 outputs encoded 'processed' data).

While Lyons teaches processor modules receiving, processing, and outputting data, Lyons does not specifically teach the **input, processing, and output as being controlled synchronously within cycles.**

Ahamed teaches the **input, processing, and output as being controlled synchronously within cycles** (Fig. 7 clock 21 which controls the data transfers of the processors by the unit of clock cycles).

It would have been obvious to add the synchronous behavior of Ahamed to the system of Lyons. The motivation for doing so would have been to coordinate data transfers between modules of differing processing speeds better than asynchronously (col. 3 lines 3-8). Other advantages of synchronous – clock driven – processor modules are well known in the art.

Regarding claim 3, which depends from claim 2 as it depends from claim 1, Ahamed further teaches **a synchronous circuit which causes data transfer for signal processor modules to occur in synchronization with clocks which are the same in phase and frequency** (Fig. 7 clk 21 causes data transfers for processor modules 11 and 12).

Regarding claim 4, which depends from claim 3 as it depends from claims 1 and 2,

Lyons further teaches **the data transfer widths between the signal processor modules are equal to each other** (in Fig. 2, Lyons suggests that the data transfer widths between modules are equal to teach other by assigning the same type, shape, and size of line on the output of module 132 – by S7 – and on the input of module 136 – by S8) **and**

Ahamed further teaches **the synchronous circuit determines the frequency of the transfer clock on the basis of the data transfer rate between the pair of signal processor modules between which the largest amount of data is to be transferred** (Ahmed teaches the determination of clk frequency based on the data transfer rate of the slow processor 11; by adding the synchronization features of Ahamed to the module transfers of Lyons as discussed in the rejection of claim 2, the determination of the clock frequency would be based on the speeds of the processor modules 132 and 136 and the amount of data between them, which would have been obvious to one of ordinary skill in the art).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lyons and Durkos et al. (US 4777590) hereafter referred to ask Durkos.

Regarding claim 5, which depends from claim 1, Lyons teaches all of the limitations of claim parent claim 1 as discussed above.

While Lyons teaches a system with multiple functional modules for performing computing tasks, Lyons does not specifically teach **a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules and a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component rearward of the signal processor module when it is not mounted on the mounting means.**

Durkos teaches a system with multiple functional modules for performing computing tasks including:

a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules (Fig. 4, wherein the modules 102 can be removably plugged-in 'mounted' in the system) **and**

a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component forward of the signal processor module when it is not mounted on the mounting means (Fig. 4, wherein module select circuit 56 acts as a switching means by switching which plugged-in 'mounted' modules 102 are connected to each other in the system, and when a module is not plugged-in to the system, data is routed to the next module).

It would have been obvious to one of ordinary skill in the art to provide a system with the modules of Lyons that are mountable as in Durkos. Durkos teaches that the modules are in series (wherein the block arrows between modules signify connections in Fig. 4) and teaches modules with different functionalities. It would have been obvious to one of ordinary skill that a module in Durkos could have been an encoding or decoding module such as in Lyons. The motivations for doing so would have been to provide for an easily customizable and upgradeable system (Durkos col. 1 lines 51-52).

Conclusion

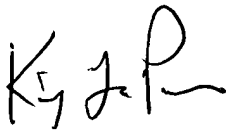
7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucas Divine whose telephone number is 571-272-7432. The examiner can normally be reached on Monday - Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lucas Divine

KING Y. POON
PRIMARY EXAMINER

Examiner
Art Unit 2624

ljd